The M68000 Family

. . . the Upward Compatible 8–/16–/32–Bit Microprocessor Family

In Brief . . .

An MPU For All Functions

To designers of the most advanced microcomputer systems, the Motorola M68000 Family of microprocessors needs no introduction. Products based on its members have become the standard for systems utilizing the UNIX operating system and for CAD/CAM engineering workstations. They are invading the next generation designs of personal computers and color graphics systems, and they find widespread implementation in multi–user/multi–tasking applications and in small business systems. M68000 MPUs are found in the leading products in fault–tolerant systems requiring high performance and parallel processing, and they are the preferred components for artificial intelligence engines requiring large linear addressing capabilities. Control applications include graphics, numerical controllers, robotics, telecommunications switching and PBX voice/data transmission.

Upward Compatibility

The M68000 MPU Family consists of a line of processors based on a 32–bit flexible register set, a large linear address space, a simple yet powerful instruction set and flexible addressing modes. The internal architecture of the 8–, 16–, and 32–bit MPU versions, and the common instruction set, provide software compatibility and offer an easy upward migration path for products requiring increasing levels of processing power.

A Host of Peripherals

A large selection of full–function peripheral chips complements the processor family. Compatible LSI and VLSI chips for memory management, data communications, DMA control, network control, system interfacing, general I/O and graphics, all simplify system design and reduce design and manufacturing cost while improving system performance.

Microprocessors

The 68K Family of Microprocessors has revolutionized virtually every segment of the electronic industry. They have set the standard for performance while still maintaining binary software compatibility from generation to generation. The combination of low cost and high performance (measured in $/system MIPS) makes every member of the Family a price performance leader. The M68000 Family provides the widest range of price and performance with choices from 1.6 MIPS to over 100 MIPS.

Table 1.

	68000	68020	68030	68040	68060
MIPS	1.6	5.5	12	35	100
MFLOPS	–	0.25	0.5	3.5	12
Address Range	16M Byte	4G Byte	4G Byte	4G Byte	4G Byte
Data Bus	16 bit	32 bit	32 bit	32 bit	32 bit
Clock Speed (MHz)	8–16	16–33	16–50	25–40	50–66
Instruction Cache	–	256 Byte	256 Byte	4K Byte	8K
Data Cache	–	–	256 Byte	4K Byte	8K
Burst Mode	–	–	16 Byte R	16 Byte R/W	16 Byte R/W
General Purpose Registers	16	16	16	16	16
Address Modes	14	18	18	18	18
On–Chip MMU	No	No	Yes	Yes*	Yes*
Floating–Point Solution	68881	68882	68882	On–Chip	On–Chip

*Separate Instruction/Data

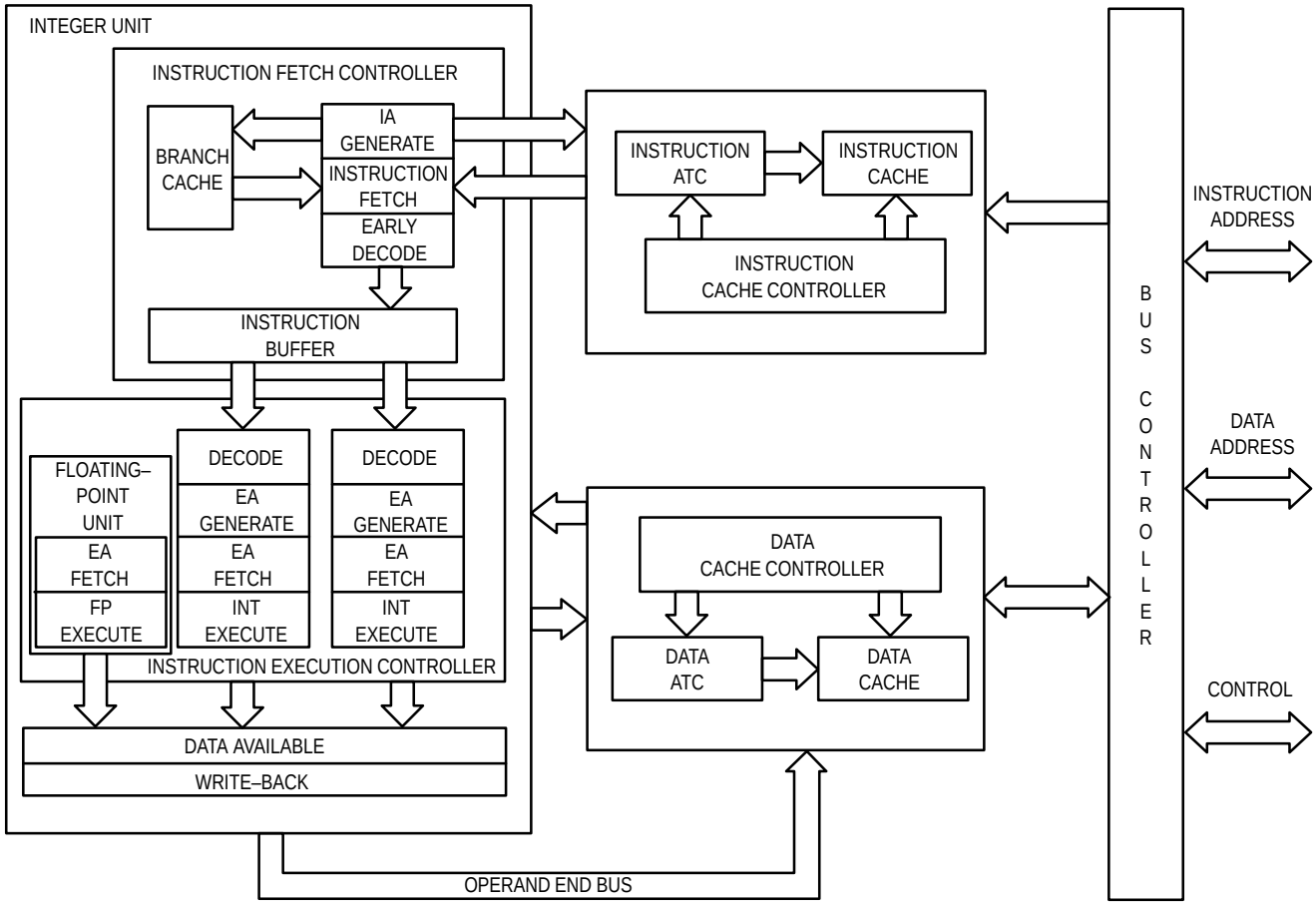

Figure 1. MC68060 Block Diagram

MC68060
Superscalar 32–Bit Microprocessor

The MC68060 is fully compatible with all previous members of the M68000 family. The MC68060 features dual on–chip caches, fully independent demand–paged memory management units (MMUs) for both instructions and data, dual integer execution pipelines, on–chip floating–point unit (FPU) and a branch target cache. A high degree of instruction execution parallelism is achieved through the use of a full internal Harvard architecture, multiple internal buses, independent execution units, and dual instruction issue within the instruction controller. Power management is also a key part of the MC68060 architecture. The MC68060 offers a low–power mode of operation that is accessed through the LPSTOP instruction, allowing for full power–down capability. The MC68060 design is fully static so that when circuits are not in use, they do not draw power. Each unit can be disabled so that power is used only when the unit is enabled and executing an instruction.

Complete code compatibility with the M68000 family allows the designer to draw on existing code and past experience to bring products to market quickly. There is also a broad base of established development tools, including real–time kernels, operating systems, languages and applications, to assist in product design. The functionality provided by the MC68060 makes it the ideal choice for a range of high–performance computing applications as well as many portable applications that require low power and high performance.

MC68040
Third–Generation 32–Bit Microprocessor

The MC68040 is Motorola's third generation of M68000–compatible, high–performance, 32–bit microprocessors. The MC68040 is a virtual memory microprocessor employing multiple, concurrent execution units and a highly integrated architecture to provide very high performance in a monolithic HCMOS device. On a single chip, the MC68040 integrates an MC68030–compatible integer unit, an IEEE 754–compatible floating–point unit (FPU), and fully independent instruction and data demand–paged memory management units (MMUs), including independent 4K–byte instruction and data caches. A high degree of instruction execution parallelism is achieved through the use of multiple independent execution pipelines, multiple internal buses, and a full internal Harvard architecture, including separate physical caches for both instruction and data accesses. The MC68040 also directly supports cache coherency in multimaster applications with dedicated on–chip bus snooping logic.

The MC68040 is an enhanced, 32–bit, HCMOS microprocessor that combines the integer unit processing capabilities of the MC68030 microprocessor with independent 4K–byte data and instruction caches and an on–chip FPU. The MC68040 maintains the 32–bit registers available with the entire M68000 Family as well as the 32–bit address and data paths, rich instruction set, and versatile addressing modes. Instruction execution proceeds in parallel with accesses to the internal caches, MMU operations, and bus controller activity. Additionally, the integer unit is optimized for high–level language environments. The MC68040 is user–object–code compatible with previous members of the M68000 Family and is specifically optimized to reduce the execution time of compiler–generated code. The MC68040 is implemented in Motorola's latest HCMOS technology, providing an ideal balance between speed, power, and physical device size.

Instruction execution is pipelined in both the integer unit and FPU. Independent data and instruction MMUs control the main caches and the address translation caches (ATCs). The ATCs speed up logical–to–physical address translations by storing recently used translations. The bus snooper circuit ensures cache coherency in multimaster and multiprocessing applications. The MC68040 FPU is user–object–code compatible with the MC68882 floating–point coprocessor. The FPU has been optimized to execute the most commonly used subset of the MC68882 instruction set, and includes additional instruction formats for single– and double–precision rounding of results.

The MMUs support multiprocessing, virtual memory systems by translating logical addresses to physical addresses using translation tables stored in memory. Each MMU has two transparent translation registers available that define a one–to–one mapping for address space segments ranging in size from 16 Mbytes to 4 Gbytes each. The instruction and data caches operate independently from the rest of the machine, storing information for fast access by the execution units. Each cache resides on its own internal address bus and internal data bus, allowing simultaneous access to both. The data cache provides writethrough or copyback write modes that can be configured on a page–by–page basis.

The MC68040 bus controller supports a high–speed, nonmultiplexed, synchronous external bus interface, which allows the following transfer sizes: byte, word (2 bytes), long word (4 bytes), and line (16 bytes). Line accesses are performed using burst transfers for both reads and writes to provide high data transfer rates.

MC68030
The Second Generation 32–Bit MPU

The 030 started with a high performance 020 core and added many performance improvement features including increased internal parallelism, dual on–chip caches with a burst fillable mode, dual internal data and address buses, improved bus interface, and on–chip paged memory management unit.

Two independent 32–bit address buses and two 32–bit data buses allow the CPU, caches, MMU, and the bus controller to operate in parallel, so the 030 can, for example, simultaneously access an instruction from the instruction cache, data from the data cache and instruction/data from external memory.

Performance is further enhanced by on–chip instruction and data caches. Separate 256–byte data and instruction caches reduce the access time and increase CPU throughput by providing data and instructions on–chip.

Overall bus requirements are reduced and multiple processors can run more efficiently thanks to increased bandwidth of the 030 bus, achieved by the enhanced bus controller allowing high speed fills of both data and instruction caches.

The on–chip paged memory management unit translates logical address to the corresponding physical address in 1/2 the time required by the 020 and MC68851 Paged Memory Management Unit. Pipelining permits this translation to be performed in parallel with other functions so that no translation time is added to any bus cycle.

MC68020

The Original 32–Bit Performance Standard

The MC68020, oh twenty, is the industry's leading 32–bit microprocessor because of high performance, architecture, ease of design–in, and long–range compatible growth path.

The 020 has a full 32–bit internal and 32–bit external, regular, symmetrical architecture designed with the customer in mind. It offers all the functionality of the other M68000 Family MPUs, and maintains software user–code compatibility which controls the expense of your product migration.

Programmers appreciate the large general purpose register set, simple yet powerful instruction set and the many flexible M68000 addressing modes. The unique on–chip instruction cache helps provide burst–mode operation to 12.5 MIPS.

The 020 is the proven leader in high performance systems in office automation, engineering workstations, fault tolerant computers, parallel processors, telephone switching systems, and intelligent controllers.

MC68010

A Virtual Memory Enhancement

The MC68010 offers the advantage of Virtual Memory. A high–speed loop mode operation executes tight software loops faster to enhance performance. Its instruction continuation feature has made it the choice for fault–tolerant and parallel processing systems. The MC68010 can support a governing operating system which handles the supervisory chores of any number of subordinate operating systems.

MC68HC000

A Micropower Alternative

HCMOS design gives the MC68HC000 all the functions and performance of its MC68000 predecessors . . . at one–tenth of the operating power requirements. With a maximum power dissipation of only 0.175 watts, the MC68HC000 is ideal for high–performance computer peripherals, industrial controllers, instrumentation and communications equipment.

MC68HC001

Low Power HCMOS 8–/16–/32–Bit Microprocessor

The MC68HC001 provides a functional extension of the MC68HC000 HCMOS 16–/32–bit microprocessor with the addition of statically selectable 8– or 16–bit data bus operation. The MC68HC001 is object–code compatible with the MC68HC000, and code written for the MC68HC001 can be migrated without modification to any member of the M68000 Family. This is possible because the user programming model is identical for all members of the M68000 Family and the instruction sets are proper subsets for the complete architecture.

MC68000

The 16–Bit Foundations

As the first member of the M68000 family, the state–of–the–art technology and advance circuit design concepts of the MC68000 16–bit MPU started a new trend in microprocessor architecture. Its seventeen 32–bit data and address registers permit rapid internal execution of its powerful yet simple instruction set. It is designed for large multiprocessing systems and realtime applications with vectored interrupts, seven priority levels and a 16 megabyte linear addressing space. It offers mainframe–like performance, supporting high–level languages and sophisticated operating systems.

The MC68000 MPU has been joined by more advanced products with even greater capabilities, yet it satisfies a large segment of the existing applications. It is extremely cost competitive and it remains one of the major growth products in the entire MPU line.

MC68008

An 8–Bit Compatible Competitor

With an 8–bit data bus and 32–bit internal architecture, the MC68008 offers performance that competes with a number of 16–bit MPUs. It has the same register set, same instructions, and the same functionality as the MC68000 with extensive exception processing. Large modular programs can be developed and executed efficiently because of the large, 1–megabit non–segmented, linear address space. It is the choice for high performance, cost effective, 8–bit designs, particularly those requiring a migration path to 16–bit or full 32–bit operation.

Embedded Controllers

The principle elements of this popular microprocessor family have now been redesigned specifically for embedded applications. The new 68EC0x0 family including the 68EC000, EC020, EC030 and EC040 MPUs are all optimized for cost–sensitive embedded control designs. The 68EC0x0 family offers the high performance of the 680x0 family, yet streamlines the feature sets for embedded applications. The 68EC0x0 family completes the triad forming the M68000 family of compatible products: the 680x0 family of computer–class central processing units; the 68300 family of integrated processors; and now, the 68EC0x0 family of embedded microprocessors.

Table 2.

	68EC000	68EC020	68EC030	68EC040/ LC040	68040V	68EC060/ LC060
MIPS	2.5	6.5	10.7	44	44	100
Address Range	16M Byte	16M Byte	4G Byte	4G Byte	4G Byte	46
Data Bus	16 bit	32 bit	32 bit	32 bit	32 bit	32 bit
Clock Speeds	8, 10, 12, 16 MHz	16, 25 MHz	25, 40, 50 MHz	20, 25, 33, 40 MHz	25, 33, 40 MHz	50, 60 MHz
Instruction Cache	–	256 Byte	256 Byte	4K Byte	4K Byte	8K Byte
Data Cache	–	–	256 Byte	4K Byte	4K Byte	8K Byte
Burst Fill Caches	–	–	16 Bytes	16 Bytes	16 Bytes	16 Bytes
General Purpose Registers	16	16	16	16	16	16
Address Modes	14	18	18	18	18	18
Floating Point Hardware	68881/68882	68881/68882	68881/68882	None	None	None
Packages	PLCC	PPGA, PQFP	PPGA, CQFP	PGA, CQFP	PGA, CQFP	PGA, CQFP

MC68EC/LC060

32–Bit High–Performance Embedded Controller

The 68EC060 is the newest addition to Motorola's embedded microprocessor family. It is the performance leader for top of the line embedded applications. The 68EC/LC060 offers 100 MIPS performance while maintaining complete backward compatibility with the 680x0 family. The 68LC060 offers a paged memory management unit while the 68EC060 has been optimized for embedded systems requiring lower–cost performance.

MC68EC040

32–Bit High–Performance Embedded Controller

The EC040 is capable of delivering 44 MIPS of sustained performance with a system cost that is unattainable by competing architectures. The LC040 offers all the features of the EC040 plus adds a paged memory management unit allowing more sophisticated operating systems features, including better memory protection.

This impressive performance is a result of a six–level pipelined integer unit, independent four–way set–associative instruction and data caches, and a very high level of on–chip parallelism. The EC040 also supports multimaster and multiprocessor systems with bus snooping.

By integrating all these features into the EC040, the microprocessor is able to perform the vast majority of work on–chip, limiting external memory accesses to allow for higher system performance with less expensive DRAMs. The result is virtual immunity to the effects of memory wait states.

MC68040V

Low–Power 32–Bit Embedded Controller

The 68040V is a low–power version of the MC68LC040. Using advanced static design techniques and 3.3 Volt supply, this part offers all the performance and features of the LC040, but requires much less power. The 040V instruction set is fully 040 compatible, but adds a low–power STOP instruction to allow for software power–down of the processor to save power.

MC68EC030

32–Bit Enhanced Embedded Controller

The MC68EC030 is a 32–bit embedded controller that streamlines the functionality of an MC68030 for the requirements of embedded control applications. The MC68EC030 is optimized to maintain performance while using cost–effective memory subsystems. The rich instruction set and addressing mode capabilities of the MC68020, MC68030, and MC68040 have been maintained, allowing a clear migration path for M68000 systems. The MC68EC030 is object–code compatible with the MC68020, MC68030, and earlier M68000 microprocessors. Burst–mode bus interface is provided for efficient DRAM access.

The MC68EC030 has an on–chip data cache and on–chip instruction cache with 256 bytes each. Dynamic bus sizing is available for direct interfacing to 8–, 16–, and 32–Bit Devices. The MC68EC030 includes 32–bit nonmultiplexed address and data buses, sixteen 32–bit general–purpose data and address registers, and two 32–bit supervisor stack pointers and eight special–purpose control registers. The EC030 provides complete support for coprocessors with the M68000 coprocessor interface. There are two access control registers that allow blocks to be defined for cacheability protection. The pipelined architecture, along with increased parallelism, allows internal caches accesses in parallel with bus transfers and overlapped instruction execution. The enhanced bus controller supports asynchronous bus cycles (three clocks minimum), synchronous bus cycles (two clocks minimum), and burst data transfers (one clock).

MC68EC020

32–Bit Embedded Controller

The 68EC020, with a complete 32–bit internal implementation, has a 32–bit data bus and an on–chip instruction cache to provide dramatically increased performance over 8– and 16–bit microprocessors. In addition, upward migration to the EC020 is made simple with dynamic bus sizing, allowing 8, 16 and 32–bit peripherals to communicate with the microprocessor.

Other performance features include advanced bit manipulation capabilities that provide multiple bit shift operations in a single instruction cycle. This capability greatly simplifies and accelerates the bit operations required in graphics processing and optical recognition applications.

MC68EC000

Low–Powered HCMOS Embedded Controller

The 68EC000 is a low–power HCMOS derivative of the 68000 optimized for cost–effective embedded processing. The EC000 has a flexible data bus that can operate in either 8– or 16–bit modes and a 24–bit address bus that provides 16 Mbytes of memory addressing capability. Electrical characteristics of the 68EC000 have been optimized to ensure easy access to low–cost memories.

The 68EC000 represents the lowest cost entry point to any 32–bit architecture. Coupled with efficient support for high–level languages and real–time operating systems, the 68EC000 provides unparalleled compatible migration paths to higher performance.

Integrated Processors

Powerful solutions to cost–, space–, and power–sensitive embedded applications are provided by the 68300 family of integrated microprocessors and microcontrollers. The 68300 family combines two of Motorola's greatest strengths — the 32–bit microprocessor architecture of the 68000 family and a proliferation of peripheral circuits offering a growing family of integrated solutions.

The 68000 family is based on a proven, expandable architecture that spans the performance range from 1 to over 29 MIPS. This architecture offers the industry's highest level of compatibility for both hardware and software. Motorola's single–chip microcomputers and microcontrollers provide the industry's broadest selection of peripheral combinations, insurance that one will fit the need of practically any application. The 68300 family embraces both of these concepts.

Each member of the 68300 family contains a core processor based on the 68000 family, a System Integration Module (SIM), an on–chip bus and various peripheral modules. The SIMs include support circuitry such as clock generation, external chip selects, system protection, timers and JTAG. The on–chip intermodule bus (IMB) on the CPU32–based 68300s creates a standard interface over which the CPU and each of the modules communicate. The peripheral modules include specialized processors, system controllers, traditional peripherals and memory. Because the peripheral modules are independent from each other, they can appear in multiple 68300 devices. With so many major features incorporated into a single 68300 device, a system designer can realize improved reliability along with significant savings in design time, power consumption, cost, board space, pin count and program development. In a 68300 device, the major functions and glue logic are all properly connected, internally timed with the same fast clock, fully tested and consistently documented.

Table 3.

	68302	**68306**	**68330**	**68331**	**68332**	**68333**	**68334**	**68340**	**68307**	**68322**	**68328**
Core Processor	68000	68EC00	CPU32	CPU32	CPU32	CPU32	CPU32	CPU32	EC000	EC000	EC000
Speeds (MHz)	16, 20	16, 20	16, 25	16	16	16	16	16, 25	16	16, 20	–
DMA	Yes	–	–	–	–	–	–	Yes	–	Yes	–
Serial Processor	Yes	–	–	–	–	–	–	–	–	–	–
Time Processor Unit	–	–	–	–	Yes	Yes	Yes	–	–	–	–
Flash EEPROM	–	–	–	–	–	64K	–	–	–	–	–
Serial I/O	Yes	Yes	–	Yes	Yes	Yes	–	Yes	Yes	–	Yes
Timers	1	–	–	1	–	–	–	2	2	1	2
A/D Converter	–	–	–	–	–	Yes	Yes	–	–	–	–
SRAM	1K	–	–	–	2K	4K	1K	–	–	–	–
DRAM Controller	–	Yes	–	–	–	–	–	–	–	Yes	–
Glue Logic (SIM)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
3.3 Volts Available	–	–	–	–	–	–	–	Yes	Yes	–	Yes
Graphic Processor	–	–	–	–	–	–	–	–	No	Yes	No

MC68302

Integrated Multiprotocol Processor

The MC68302 integrated multiprotocol processor (IMP) is a very large–scale integration (VLSI) device incorporating the main building blocks needed for the design of a wide variety of controllers used in the communications industry. The IMP is the first device to offer the benefits of a closely coupled, industry–standard M68000/MC68008 microprocessor core and a flexible communications architecture. The three–channel communications device may be configured to support a number of popular industry interfaces, including those for the Integrated Services Digital Network (ISDN) basic rate and terminal adaptor applications. Through a combination of architectural and programmable features concurrent operation of different protocols (HDLC/SDLC™, UART, BISYNC, DDCMP™, or transparent modes) can easily be achieved. Data concentrators, modems, line cards, bridges, and gateways are examples of suitable applications for this device.

The IMP is a Complementary Metal–Oxide Semiconductor (CMOS) device consisting of an M68000/MC68008 microprocessor core, a system integration block (SIB), and a Communications Processor (CP). By integrating the microprocessor core with the serial ports (in the CP) and the system peripherals (in the SIB), the IMP is capable of handling complex tasks such as all ISDN basic rate (2B+D) access tasks.

MC68306

Integrated 68EC000 Processor

The 68306 integrated EC000 processor includes many of the features commonly found in 68000–based designs. The 68306 includes a 68EC000 core processor, a 68681 Dual Universal Asynchronous Receiver Transmitter (DUART), system integration functions, and a DRAM controller. The on–chip DRAM controller gives the 68306 the family's simplest interface to DRAM–based designs. The DRAM controller easily accommodates 64 Mbytes of memory. The 68306 saves time in the design cycle by providing valuable 68000 system components pre–packaged in one chip.

MC68307

Integrated EC000 Processor

The 68307 is an integrated processor combining a static EC000 processor with multiple inter–chip bus interfaces. The 68307 is designed to provide optimal integration and performance for applications such as digital cordless telephones, portable measuring equipment, and POS terminals. By providing 3.3 V, static operation in a small package, the 68307 delivers cost effective performance to handheld battery–powered applications.

MC68322

Integrated EC000 Printer Processor

The 68322 is a high–performance integrated printer processor that combines a 68EC000 core, a RISC graphics processor, a print engine video controller and numerous system integration features on a single integrated circuit. It is the first of Motorola's M68000 family designed specifically for pinters. The 68322 provides a unique solution for new designs as well as an excellent migration path for existing M68000–powered printers.

MC68328

Integrated EC000 Processor

The 68328 processor provides key features that are suitable for many portable applications. Modules like a real–time clock, LCD controller, pulse–width modulator, timers, master and slave serial peripheral interface, UART and system integration give the engineer more flexibility and resource to design efficient and innovative products.

MC68330

Integrated CPU32 Processor

The 68330 is ideal for applications requiring 32–bit microprocessor performance without the additional expense inherent in 32–bit memory systems. The 68330 is the simplest and lowest priced member of the CPU32–based 68300 family. The 68330 allows the designer access to the high performance of the CPU32 along with minimized external glue logic, while allowing the greatest freedom in selecting needed peripherals, ASICs or gate arrays.

MC68331

32–Bit Microcontroller

The 68331 is well suited to applications requiring simple serial communications and general timing needs. The 68331 contains the CPU32, a SIM, a General Purpose Timer (GPT) and a Queued Serial Module (QSM). The general purpose timer is a simple yet flexible timer that provides four modes of operation with multiple channels for some operations. The QSM provides two modes of communication: an asynchronous channel that provides up to 524–Kbits per second transfer rate and a serial peripheral interface with separate 16–word receive/transmit queues.

MC68332

32–Bit Microcontroller

The 68332 is especially suited for high–performance timing applications such as automotive engine control, precision motor control and industrial robotics. The powerful Time Processor Unit (TPU) distinguishes the 68332 providing optimum performance in controlling time–related activity. It drastically reduces the need for CPU intervention with its dedicated execution unit, tri–level prioritized scheduler, data storage RAM and dual time bases. In addition to the TPU and CPU32, the 68332 features the QSM, a SIM and 2–Kbytes of standby static RAM.

MC68F333

32–Bit Microcontroller

The 68F333 provides the highest level of integration available to high–performance timing applications such as avionics and automotive engine control. The 68F333 contains the CPU32, the TPU and the QSM. It also adds two banks of flash EEPROM totaling 64–Kbytes, a total of 4–Kbytes of SRAM (512 bytes separately powered) and an 8–channel, 10–bit analog–to–digital converter. The Single–Chip Integration Module (SCIM) allows 18 of the external address and data pins to be converted to I/O pins, resulting in a single–chip solution suitable for many applications.

MC68334

32–Bit Microcontroller

The 68334 is a streamlined version of the 68332, taking advantage of the powerful TPU. The 68334 includes the CPU32 core processor, the TPU, a SIM, 1–Kbyte of SRAM, a 10–bit analog–to–digital converter and up to 47 discrete I/O lines.

MC68340

Integrated Multiprotocol Processor with DMA

The 68340 is excellent for applications requiring high–speed or block data transfers, such as disk drives and navigation systems. The combination of general peripherals and the extremely low power consumption possibilities of the 68340 make it ideal for many battery powered, portable applications such as hand held computers and data acquisition systems.

The most distinguishing 68340 feature is the high speed two channel, 32–bit Direct Memory Access (DMA) controller. Incorporating the CPU32 and DMA on the same chip eliminates the usual bus arbitration and synchronization delays, maximizing data throughout (25–Mbytes per second on a 16–bit bus).

In addition to the CPU32, a SIM and the DMA, the 68340 contains a 68681/2681–compatible DUART. The 68340 also has two identical, versatile counter/timers, each with a 16–bit counter and an 8–bit prescaler with 80 ns resolution.

Coprocessors

MC68851

Paged Memory Management Unit, PMMU

The PMMU is a 32–bit memory manager which provides full support for a demand paged virtual environment with the 68010 or MC68020. It supports a 4–gigabyte addressing space when used as a coprocessor with the MC68020. An on–chip address translation cache minimizes translation delays and maximizes system performance.

MC68881

A Floating Point Coprocessor

Designed specifically for arithmetic expansion of the MC68020 MPUI, this powerful coprocessor can also be used as a peripheral to all other M68000 family members, and with non–M68000 processors as well. It performs floating point math calculations in strict conformance to a full implementation of the IEEE Standard for Binary Floating Point Arithmetic (754) and, in addition to the basic add, subtract, multiply, and divide functions, it handles full selection of transcendental and non–transcendental operations. These operations include root values, trigonometric functions, exponentials, hyperbolics, and logs. All functions are calculated to 80 bits of extended precision in hardware.

MC68882

Enhanced Floating Point Coprocessor

The MC68882 is pin–to–pin hardware and software compatible with the MC68881 Floating Point Coprocessor and implements a variety of performance enhancements including dual–ported registers and an advanced pipeline. Additional circuitry allows execution of multiple instructions in parallel for more than twice the Floating Point performance of the trail–blazing MC68881. Where higher performance requirements indicate, the MC68882 is a drop–in replacement for the MC68881.

DMA Controllers

MC68450

DMA Controller, DMAC

The DMAC maintains high–performance data movement for complex M68000 MPU–based systems. While pin compatible with the MC68440 DDMA, the DMAC offers four completely independent DMA channels. In addition to all the features of the DDMA, the DMAC also provides very sophisticated manipulation of data through sequential and linked array–chained addressing capabilities.

MC68440

Dual Direct Memory Access Controller, DDMA

The DDMA complements the performance capabilities of M68000 microprocessors by moving blocks of data in a quick, efficient manner with a minimum of intervention from the MPU. The DDMA performs memory–to–memory, peripheral–to–memory, and memory–to–peripheral transfers through each of two completely independent DMA channels. The DDMA also offers two interrupt vectors per channel and supports both 8–bit and 16–bit data transfers.

Network Devices

MC68824

Token Bus Controller, TBC

The TBC is the industry's first single–chip VLSI device to implement the IEEE 802.4 Media Access Control Sublayer of the ISO Data Link Layer, as specified by General Motors Manufacturing Automation Protocol, MAP. The TBC supports serial data rates of 1, 5, and 10 Mbps and relieves the host processor of the frame formatting and token management functions. For efficient transfer of data frames, to and from memory, the TBC features an on–chip four–channel DMA with bus master capability, a 32–bit address range, an 8– or 16–bit data bus, and a 40–byte FIFO. The MC68824 also offers support options for network bridges, real–time support and network monitoring services.

MC68184

Broadband Interface Controller

The MC68184 Broadband Interface Controller (BIC) is a high–performance interface device for use with the MC68824 Token Bus Controller (TBC) to implement the digital portion of the physical layer of a broadband IEEE 802.4 token bus node. The BIC manipulates both data and control for RF transmitter circuitry and RF receiver circuitry. The CMOS BIC supports data rates up to 10 Mbps using a duo–binary modulation technique and provides 20 lines for receiver/transmitter control with 13 user–defined outputs.

The BIC performs the digital functions of the physical layer when implementing a broadband token bus node. The modem side of the BIC provides data and control for the RF transmitter/receiver circuitry. A standard serial interface is used to connect the BIC to the MC68824 TBC. The TBC performs the media access control (MAC) function. The MC68184 has the ability to scramble and descramble data.

MC68185
Twisted–Pair Modem

The MC68185 Twisted–Pair Modem (TPM) is used in conjunction with a MC68824 Token Bus Controller (TBC), an RS485 transceiver, and a twisted–pair media to implement a low–cost area network (LAN). The MC68824 TBC implements the layer 2 media access control (MAC) portion of the IEEE 802.4 LAN station and receiver portion for the IEEE 802.2 logical link control (LLC) type 3 as well as providing support for LLC type 1 and type 2. The TPM interfaces directly to the TBC, providing physical layer management, including MAC symbol encoding/decoding at data rates up to 2 Mbps.

The TPM contains an 32 kHz to 20 MHz on–chip crystal oscillator that generates a transmit clock without external circuitry. The physical layer management includes local loopback mode, transmitter enable, and reset. An on–chip digital filter provides for noise reduction of received data.

MC68194
Carrierband Modem

The bipolar LSI MC68194 Carrierband Modem (CBM), when combined with the MC68824 Token Bus Controller (TBC), provides an IEEE 802.4 single–channel, phase–coherent carrierband, Local Area Network (LAN) connection. The CBM performs the physical layer function, including symbol encoding/decoding, signal transmission and reception, and physical management.

The CBM provides the three basic functions of the physical layer: data transmission to the coaxial cable, data reception from the cable, and management of the physical layer. For standard data mode (also called MAC mode), the CBM receives a serial transmit data stream from the TBC (called symbols or atomic symbols), encodes, modulates the carrier, and transmits the signal to the coaxial cable. Also in the data mode, the CBM receives a signal from the cable, demodulates the signal, recovers the data, and sends the received data symbols to the TBC. End–of–transmission receiver blanking as required by IEEE 802.4 is supported. Communication between the TBC and CBM is through a standardized serial interface consistent with the IEEE 802.4 DTE–DCE interface.

MC68195
Local Talk Adaptor

The MC68195 LocalTalk adaptor (LA) is used in conjunction with the MC68302 Integrated Multiprotocol Processor (IMP) to build a network interface to LocalTalk™, also known as AppleTalk™. LocalTalk refers to the 230.4–kbps Local Area Network (LAN) that connects multiple MacIntosh™ computers and printers.

The LA provides LocalTalk support for any two of the three IMP serial channels. Combinations of multiple LA and/or IMP devices may be used to support additional LocalTalk channels. Non–LocalTalk applications can use the LA device with the IMP to build proprietary HDLC–based LANs at up to 2.5 Mbps using bi–phase space (FMO) encoding.

MC68605
X.25 Protocol Controller, XPC

The XPC implements the 1984 CCITT X.25 Recommendation Data Link Procedure (level 2) LAPB. In addition to handling the lower level communications functions (HDLC framing, CRC generation/checking, and zero insertion/deletion), the XPC also independently handles higher level communications functions (frame sequencing, retransmission, flow control, retries limit and timeout conditions). This allows the host to operate almost totally isolated from the task of ensuring error–free transmission and reception of data.

MC68606
Multi–Link LAPD Controller CCITT Q.920/Q.921, LAPD

The MC68606 Multi–link LAPD (MLAPD) Protocol Controller fully implements CCITT Recommendation Q.920/Q.921 Link Layer Access Procedure (LAPD) protocol for ISDN networks. The MLAPD is designed to handle both signalling and data links in high–performance ISDN primary rate applications.

This VLSI device provides a cost–effective solution to ISDN link–level processing with simultaneous support for up to 8K logical links. The MC68606 is an intelligent communications protocol controller compatible with AT&T specifications for ISDN devices and features low power consumption and high performance, with an aggregate data rate in excess of 2.048 Mbps.

Data Communication Devices

MC68HC681
MC68HC2681

Dual Universal Asynchronous Receiver/Transmitter, DUART

The MC68HC681 features two completely independent full–duplex asynchronous receiver/transmitter channels that interface directly to the M68000 microprocessor bus. Receiver data registers are quadruple buffered and transmitter data registers are double buffered for minimum MPU intervention. Each has its own independently selectable baud rate. Multifunction 6–bit input port and 8–bit output port, a 16–bit programmable counter/timer, interrupt handling capabilities, and a maximum one–megabyte per second transfer rate make the DUART an extremely powerful device for complex data communication applications. Full device functionality with an M6800 bus interface is provided by the MC68HC2681.

General Purpose I/O

MC68230

Parallel Interface/Timer, PI/T

The PI/T provides versatile double–buffered parallel interfaces and a system–oriented timer for M68000 systems. The parallel interfaces operate either in a unidirectional or bidirectional mode, either 8– or 16–bit wide. The timer is 24 bits with full programmability and a 5–bit prescaler. The PI/T has a complete M68000 bus interface and is fully compatible with the MC68450 DMAC.

MC68HC901

Multifunction Peripheral, MFP

The MFP provides basic microcomputer function requirements as a single companion chip to the M68000 Family of Microprocessors. Features provided via a direct M68000 system bus interface include a full–function, single–channel Universal Serial Asynchronous Receiver/Transmitter (USART) for data communication, an 8–source interrupt controller, eight parallel I/O lines, and four 8–bit timers.

Fiber Distributed Data Interface

Fiber Distributed Data Interface (FDDI) is defined as a dual fiber–optic token ring LAN (Local Area Network) that can support rates up to 100 Mbps. It can accommodate rings with 1,000 stations. Two kilometers between stations, and up to 200 kilometers in total length. This technology is driven by the need to support high performance distributed computer systems which are becoming faster and more powerful, thus imposing a greater need for network speed and bandwidth. Other uses for FDDI include backbone networks connecting Ethernet, Token Bus, and Token Ring segments and back end networks connecting high–speed peripherals. FDDI is an American National Standards Institute (ANSI) standard. Motorola's FDDI chip set includes the MC68836, MC68837, MC68838, and MC68839.

MC68836

FDDI Clock Generator

The MC68836 FDDI Clock Generator (FCG) implements part of the Physical Layer (PHY) functions of the FDDI standard including clock recovery, data recovery, and NRZI conversions. The FCG also does a five–bit parallel to serial conversion during transmission, and a serial to five–bit parallel conversion during reception. The FCG uses the five–bit parallel interface to communicate with the MC68837 device. The FCG directly connects to fiber optic modules through differential driver/receiver pins. Features include full duplex operations, 125 MHz clock recovery from incoming serial NRZI data stream, and 125 MHz transmit clock generation.

MC68837

Elasticity Buffer and Link Manager

The Elasticity Buffer and Link Manager (ELM) implements the remaining of the PHY functions of the FDDI standard including data framing, elasticity buffer, encoding, decoding, smoothing, line state detection, and repeat filter. The ELM also implements some Station Management (SMT) functions such as the Connection Management (CMT), Physical Connection Management (PCM), Physical Connection Insertion (PCI), and Link Error Monitor (LEM).

MC68838

Media Access Controller

The Media Access Controller (MAC) implements the MAC portion of the FDDI standard. The MAC protocol is the lower sub–layer of the ISO OSI data link layer and provides for fair and deterministic sharing of the physical medium, address recognition, frame check sequence generation and verification, frame insertion, frame repetition, frame removal, token generation, and certain error recovery procedures. Features on the MC68838 include independent receive and transmit data paths and state machines, bridging support including a bit order reversal option, a count and void frame bridge stripping algorithm, and CRC appendage on a per frame basis. The MAC also contains an interface to Content Addressable Memory (CAM) for individual and multicast address recognition.

MC68839

FDDI System Interface

The FDDI System Interface (FSI) is a high performance interface device which can easily connect to any bus including high speed processors, little– and big–endian busses, and multiplexed/non–multiplexed address data busses. Its primary purpose is to interface the FDDI protocol devices to the user system bus. FSI features include support for a ring buffer structure, addressing flexibility, programmable partitioned 8K bytes internal RAM for temporary data storage, two 32–bit ports, the ability to sustain up to 250 μs bus latencies, support for synchronous and asynchronous frames, and the ability to chain multiple buffers per frame.

Support Software

M68KESW–PC1

This Intermetrics software package is for the 68K Family (68000, 68008, 68HC001, 68010, 68020, 68030, 68EC030, 68040, 683xx). The MC68KESW InterTools package includes C compiler, assembler/linker, run–time libraries, and one year of support from Intermetrics.

M68040FPSP

This software provides 68040 floating point emulation of unimplemented 68881/68882 functions. Contact factory for license agreement.